科目： **計算機結構**（Computer Architecture） 

1. (10%) What are the causes that limit the growth of uniprocessor performance and motive the trend of developing multiple processors per chip in recent years?

2. (10%) Which of the following statements are true for General-purpose register (GPR) instruction architecture?

(A) One of the advantages of register-register instructions is simple code-generation
(B) The instruction count for register-register instructions is usually lower than register-memory instructions.
(C) Using registers is more efficient for a compiler than other forms of internal storage.
(D) When variables are allocated to registers, the memory traffic reduces, the program speeds up.
(E) None of the above

3. (10%) Consider the following instruction mix and clock cycle per instruction:
   - Frequency of ALU instructions: 40%
   - Frequency of data transfer instructions: 35%
   - Frequency of branch instructions: 25%
   - ALU instructions take 2 cycles, data transfer instructions take 3 cycles, branch instructions take 3 cycles.

   There are two enhancement alternatives:
   Enhancement A: reduce ALU instructions to 1 cycle.
   Enhancement B: reduce branch instructions to 2 cycles.
   Which alternative is better? Why?

4. (10%) Suppose we would like to achieve a speedup of 10 with 50 processors. What fraction of the original computation can be sequential?

5. (10%)
   (a) Please use an example to explain how loop unrolling is done.
   (b) What is a loop-carried dependence? Please give me an example of a loop code sequence that cannot be unrolled.

6. (10%) Given a 16-word two-way set associative cache with two-word blocks, for the following word address memory access: 12, 17, 18, 16, 5, 29, 19, 12, 4, 22, 23, 24, 17, 25, 26, 27, assume that LRU (Least Recently Used) is used. Calculate the number of hits.

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7. (10%) For a pipelined implementation, assume that 1/4 of the load instructions are immediately followed by an instruction that uses the result, half of the branches are miss-predicted with 1 clock cycle delay, and jumps always cause 1 clock cycle of delay. If the instruction mix is 24% loads, 20% stores, 30% ALU instructions, 20% branches, and 6% jumps. What is the average CPI?
8. (10%) In designing the memory hierarchy, please describe the positive and negative effects of increasing the cache size, associative and block size.
9. (10%) Given TLB, main memory, page table, cache and the secondary storage, please describe the procedures of a memory access by using these components.
10. (10%) When designing a low-power real-time embedded system, what control method, hardwired or microprogramming, will you prefer to use and why? In addition, how is memory hierarchy design in such a system different from the design of desktops or servers?