國立中央大學資訊工程學系 103 學年度第二學期博士班資格考試題紙

科目: 計算機結構 (Computer Architecture) 第一頁 共二頁 (page 1 of 2)

- 1 (10%) Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
 - (a) Which processor has the highest performance expressed in instructions per second?
 - (b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
 - (c) We are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?
- 2 (10%) The information of a virtual memory system is assumed to be:
 - Page size: 1024 words
 - Number of virtual pages: 8
 - Number of physical pages: 4
 - The current page table is

VPN	0	1	2	3	4	5	6	7
PPN	2	1	NULL	NULL	3	NULL	0	NULL

For the following (decimal) virtual word addresses: VA1: 57, VA2: 2048, VA3: 1025, VA4: 7748, VA5 6152, Please calculate their physical addresses are PA1, PA2, PA3, PA4, PA5.

- 3 (10%) A cache with data size 1Mbytes contains 16384 blocks and is four way set associative. The address 0x11D9A4F3 is accessed and is a hit in this cache. What is the corresponding tag value?
- 4 (10%) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way.
- 5 (10%) Can we keep pursuing the increase of clock rate of processors to improve the performance? Please describe your reasons.
- 6 (10%) What is Loop Unrolling when exploiting instruction level parallelism? What are the advantages? Explain it clearly by an example.

背面還有 Please Turn Over

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科目: 計算機結構 (Computer Architecture) 第二頁 共二頁 (page 2 of 2)

- 7 (15%) How does scoreboard deal with WAR, RAW, and WAW hazards? At which stage respectively?
- 8 (10%) What are the assumptions or hypothesis of a correlating branch predictor? How does it work?
- 9 (15%) Assume data reference: 25%, and there is only one memory port. Processor with structural hazard (Processor A) has a clock rate 1.2 times higher than the clock rate of the processor without the structural hazard (Processor B). Discard any other performance losses. Which processor is faster? How much faster?