國立中央大學資訊工程學系 112 學年度第一學期博士班資格考試題紙

科目： **計算機結構**（Computer Architecture） 第一頁 共二頁(page 1 of 2)

1. (10%) What are the advantages of PC relative address for conditional branch?

2. (10%) What is dynamic scheduling? Why is dynamic scheduling important?

3. (10%) Please explain why loop unrolling can increase instruction level parallelism. Please use an example to explain how loop unrolling is done.

4. (10%) Assume a disk subsystem with the following components and MTTF:
   20 disks, each rated at 1000000-hour MTTF
   1 SCSI controller, 1000000-hour MTTF
   1 power supply, 200000-hour MTTF
Assume that after adding one redundant power supply, the reliability of the power supply improves about 1000 times. What is the reliability improvement of the entire disk subsystem?

5. (10%) For single-cycle or multi-cycle implementation of CPU, which one is more efficient? Explain the reason why it is better.

6. (10%) Consider two different implementations of the same instruction set architecture. There are five classes of instructions: A, B, C, D, and E. The clock rate and the CPI (cycles per instruction) of each implementation are given in the following table.

	Clock Rate	CPI_A	CPI_B	CPI_C	CPI_D	CPI_E
P1	2.0G	1	2	3	5	4
P2	1.8G	3	3	3	3	3

   (1) Given a program with 10^5 instructions divided into classes: 10% Class A, 15% Class B, 40% Class C, 20% Class D, and 15% Class E. Which implementation (P1 or P2) is faster? (5 pts.)
   (2) Following (1), you are trying to improve P1 by saving 20% in the execution time. However, this leads to an increase of 15% of the average CPI. What clock rate should we have to set to achieve this time reduction? (5 pts.)

7. (15%) A 1 GHz machine can perform “jump” instruction with 1 clock cycle, “branch” instruction with 3 cycles, “arithmetic” instruction with 2 cycles, “multiply” instruction with 5 cycles, and “memory access” with 4 cycles. A program called “James” has 10% jumps, 10% branches, 50% arithmetic, 10% multiply, and 20% memory access.

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(1) What is the CPI of this program on this machine? (5 pts.)

(2) Now, if "James" executes 10^7 instructions on this machine. What is its execution time? (5 pts.)

(3) Following (2), a 6-cycle multiply-add instruction is implemented in this machine, and it can combine an arithmetic and a multiply instruction. 50% of the multiply instructions can be transferred to this multiply-add instruction in "James." What is the new CPI and the execution time if the clock period remains the same? (5 pts.)

8. (25%) About memory hierarchy

(1) Given cache, TLB, page table, main memory, and the secondary storage (disk), describe the process of memory access in a systematic way.
(10 pts.)

(2) Describe the positive and negative effects of increasing (a) cache size, (b) associativity, and (c) block size on the overall performance of memory access. (10 pts.)

(3) Find the average memory access time (AMAT) with a 1 ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.08 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.
(5 pts.)