國立中央大學資訊工程學系 111 學年度第二學期博士班資格考試題紙

科目： **計算機結構** （Computer Architecture） 第一頁 共二頁(page 1 of 2）

1. (10%) Suppose you want to achieve a speedup of 5 with 10 processors. At most what fraction of the original computation can be sequential?

2. (10%) Computer A can execute more instructions within a second compared to computer B. Is it proper to conclude that the performance of computer A is better than computer B? Why or why not?

3. (10%) What are the advantages of PC relative address for conditional branch?

4. (10%) (a) How many entries are in a (4,2) correlating predictor with a total of 128K bits in the branch prediction buffer?

(b)How many lower order address bits are used to index the branch prediction buffer?

5. (10%) Consider the following instruction mix and clock cycle per instruction:

☐ Frequency of ALU instructions: 40%

☐ Frequency of data transfer instructions: 30%

☐ Frequency of branch instructions: 30%

☐ ALU instructions take 2 cycles, data transfer instructions take 3 cycles, branch instructions take 3 cycles.

There are two enhancement alternatives:

Enhancement A: reduce ALU instructions to 1 cycle.

Enhancement B: reduce branch instructions to 2 cycles.

Which alternative is better? Why?

6. (10%) Describe the differences of memory design for a server and an embedded system.

背面還有 Please Turn Over

7. (30%) About memory hierarchy

(1) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way. (10 pts.)

(2) Describe the possible positive and negative effects of increasing (a) cache size, (b) associativity and (c) block size to the overall performance of memory access. (10 pts.)

(3) In a 3-level memory hierarchy system, the hit time for each level is
T1=10ns (L1-cache)
T2=200ns (L2-cache)
T3=600ns (Main memory)
The local hit rate in each level is H1=0.9 (L1-cache), H2=0.8 (L2-cache), and H3=1. (It is assumed that we can always find the data in main memory.) What is the average access time (in ns) of this memory system? (10 pts.)

8. (10%) Consider two different implementations of the same instruction set architecture. There are five classes of instructions, A, B, C, D and E. The clock rate and the CPI of each implementation are given in the following table.

	ClockRate	CPI of A	CPI of B	CPI of C	CPI of D	CPI of E
P1	2.2G	1	2	3	4	5
P2	1.8G	3	3	3	3	3

(1) Given a program with 10^6 instructions divided into classes as follows: 10% Class A, 15% Class B, 30% Class C, 25% Class D and 20% Class E. Which one (P1 or P2) is faster? (5 pts.)

(2) Following (1), you are trying to improve P1 by saving 20% in the execution time. However, this leads to an increase of 15% of the average CPI. What clock rate should we have to set to achieve this time reduction? (5 pts.)