1. (10%) A 1 GHz machine can perform "jump" instruction with 1 clock cycle, "branch" instruction with 3 cycles, "arithmetic" instruction with 2 cycles, "multiply" instruction with 5 cycles and "memory access" with 4 cycles. A program called "James" has 10% jumps, 10% branches, 50% arithmetic, 10% multiply and 20% memory access.
   (1) If "James" executes 10^7 instructions on this machine. What is its execution time? (5 pts.)
   (2) Following (2), a 6-cycle multiply-add instruction is implemented in this machine and it can combine an arithmetic and a multiply instruction. 50% of the multiply instructions can be transferred to this multiply-add instruction in "James". What is the new CPI and the execution time if the clock period remains the same? (5 pts.)

2. (20%) About memory hierarchy
   (1) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way.
   (10 pts.)
   (2) Find the average memory access time (AMAT) with a 1 ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.08 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.
   (5 pts.)
   (3) As in (4), suppose we can improve the miss rate to 0.05 misses per reference by doubling the cache size. This causes the access time to increase to 1.8 cycles. Using the AMAT as the metric, please determine if this is a good trade-off. (5 pts.)

3. (20%) For the cache memory design:
   (1) Please design a 2-way set-associative cache of 8K bytes data. The block size is 2 words with 4 bytes in each word. Assume that the total cacheable physical memory is 16MB bytes. Please show the physical address format (in the order of tag, index and offset from MSB to LSB) and then the block diagram of the design, including tags, data and valid bits. (10 pts.)
   (2) Continue (1). Here is a series of physical address references given as byte addresses:

Label	Memory address
A	0x245625
B	0x245627
C	0x245628
D	0x321620
E	0x322623
F	0x245627
G	0x245630
H	0x322622

Assume that the cache is initially empty and LRU (Least Recently Used) replacement is adopted. Determine each reference (A~H) in the list as a hit or a miss and show the final content of the cache (i.e. the non-empty set number and the stored address range).
(10 pts.)

4. (10%) Assume a disk subsystem with the following components and MTTF:
   20 disks, each rated at 1000000-hour MTTF
   1 SCSI controller, 1000000-hour MTTF
   1 power supply, 200000-hour MTTF
   Assume that after adding one redundant power supply, the reliability of the power supply improves about 1000 times. What is the reliability improvement of the entire disk subsystem?

5. (10%) Explain the concept of delay branch and different strategies to fill the delay slots.

6. (10%) For single-cycle or multi-cycle implementation of CPU, which one is more efficient? Explain the reason why it is better.

7. (10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 8 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?
   MUL F6, F5, F6
   SUB F2, F7, F8
   DIV F10, F6, F5
   ADD F5, F8, F2

8. (10%) What is a loop-carried dependence? Is it possible to perform loop unrolling when there is a loop-carried dependence? What are the conditions when performing loop unrolling is possible and impossible for a loop with a loop-carried dependence, respectively?