國立中央大學資訊工程學系 109 學年度第二學期博士班資格考試題紙

科目：**計算機結構**（Computer Architecture） 第一頁 共一頁(page 1 of 1)

1.(10%) What is dynamic scheduling? Why is dynamic scheduling important?

2.(10%) What are the causes that limit the growth of uniprocessor performance and motive the trend of developing multiple processors per chip in recent years?

3.(10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 8 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?

MUL F6, F5, F3
ADD F2, F7, F6
DIV F10, F6, F5
SUB F5, F8, F2

4.(10%) Please explain why loop unrolling can increase instruction level parallelism. Please use an example to explain how loop unrolling is done.

5.(10%) For a (2,3) correlating branch predictor, how many branch-selected entries are there in the predictor with a total 256K bits in the prediction buffer. How many bits from the last bits of branch address are used to select the prediction entries?

6.(20%) One 1 GHz machine can perform “jump” instruction with 1 clock cycle, “branch” instruction with 3 cycles, “arithmetic” instruction with 2 cycles, “multiply” instruction with 5 cycles and “memory access” with 4 cycles. A program called “Lightening” has 10% jumps, 10% branches, 50% arithmetic, 10% multiply and 20% memory access instructions.

(a) What is the CPI of this program on this machine? (6 pts.)

(b) Now, if “Lightening” executes 10^8 instructions on this machine. What is its execution time? (6 pts.)

(c) Following (b), a 6-cycle multiply-add instruction is implemented in this machine and it can combine an arithmetic and a multiply instruction. 50% of the multiply instructions can be transferred to this multiply-add instruction in “Lightening”. What is the new CPI and execution time if the clock period remains the same? (8 pts.)

7.(10%) Given the cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way.

8.(10%) A cache with data size 1Mbytes contains 65536 blocks and is 8-way set associative. The (byte) address 0x13F2B312 is accessed and is a hit in this cache. What data, i.e., the range of memory address, will surely be found in the cache? What is its “tag”?

9.(10%) In memory hierarchy, please describe the positive and negative effects of
(a) increasing cache size (b) increasing associativity (c) increasing block size.