國立中央大學資訊工程學系 108 學年度第一學期博士班資格考試題紙

科目： **計算機結構** （Computer Architecture）第一頁　共二頁(page 1 of 2）

1. (10%) Please use a figure to illustrate a (3,2) predictor selected by the lower order 10 bits of branch address and explain how it works in details. How many bits are required in this predictor?

2. (10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 8 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?
   MUL F6, F5, F6
   SUB F2, F7, F8
   DIV F10, F6, F5
   ADD F5, F8, F2

3. (10%)
   Compute the clock cycle per instruction (CPI) for the following instruction mix. The mix includes 25% loads, 18% stores, 40% R-format operations, 15% branches, and 2% jumps. The number of clock cycles for each instruction class is listed as follows. 5 cycles for loads, 4 cycles for stores, 4 cycles for R-format instructions, 4 cycles for branches, 3 cycles for jumps.

4. (10%) Suppose we would like to achieve a speedup of 10 with 50 processors. What fraction of the original computation can be sequential?

5. (10%)
   Consider the following code sequence.

```
for (i=1; i<=100; i=i+1){
        Z[i] = X[i] / c;        /*S1*/
        X[i] = Z[i] +c;         /*S2*/
        Z[i] = X[i] + c;        /*S3*/
        Y[i] = c – Y[i-1];      /*S4*/
  }
```

   (a) Find all the true dependences, output dependences, and anti-dependences
   (b) Is there a loop-carried dependence?

背面還有 Please Turn Over

6. (10%) True of False (A wrong answer will cause 1 more point loss)
   (a) A common way of presenting computer performance in a benchmark is to normalize execution times to a reference computer. Then the arithmetic mean is usually used to ensure that the performance evaluation will not be affected by using different reference machines.
   (b) In the history of computers' development, the size of memory and number of registers in a computer grow according to the Moore's law.
   (c) For a big-endian machine, if we write a 32-bit (4-byte) data word, 0xABCDEFBA, to the address 0x8000, the byte at 0x8000 is 10101011.
   (d) Tera bytes indicate 2^{40} bytes. Two Pico seconds indicate $2x10^{-12}$ seconds.
   (e) Translation Lookaside Buffer is a cache.

7. (10%)
   A 2 GHz machine can perform “jump” instruction with 1 clock cycle, “branch” instruction with 3 cycles, “arithmetic” instruction with 2 cycles, “multiply” instruction with 5 cycles and “memory access” with 4 cycles. A program called “Star” has 10% jumps, 10% branches, 50% arithmetic, 10% multiply and 20% memory access.
   (a) What is the CPI of this program on this machine?
   (b) Now, if “Star” executes 10^8 instructions on this machine. What is its execution time?
   (c) Following (b), a 6-cycle multiply-add instruction is implemented in this machine and it can combine an arithmetic and a multiply instruction. 50% of the multiply instructions can be transferred to this multiply-add instruction in “Star”. What is the new CPI and execution time if the clock period remains the same?

8. (10%) Given TLB, main memory, page table, cache and the secondary storage, please describe the procedures of a memory access by using these components.

9. (10%) A cache with data size 1Mbytes contains 8192 blocks and is two way set associative. The address 0x32E6A2AF is accessed and is a hit in this cache. What is the corresponding tag value?

10. (10%) Can we keep pursuing the increase of clock rate of processors to improve the performance? Please describe your reasons.