科目： **計算機結構** （Computer Architecture） 第一頁 共二頁(page 1 of 2)

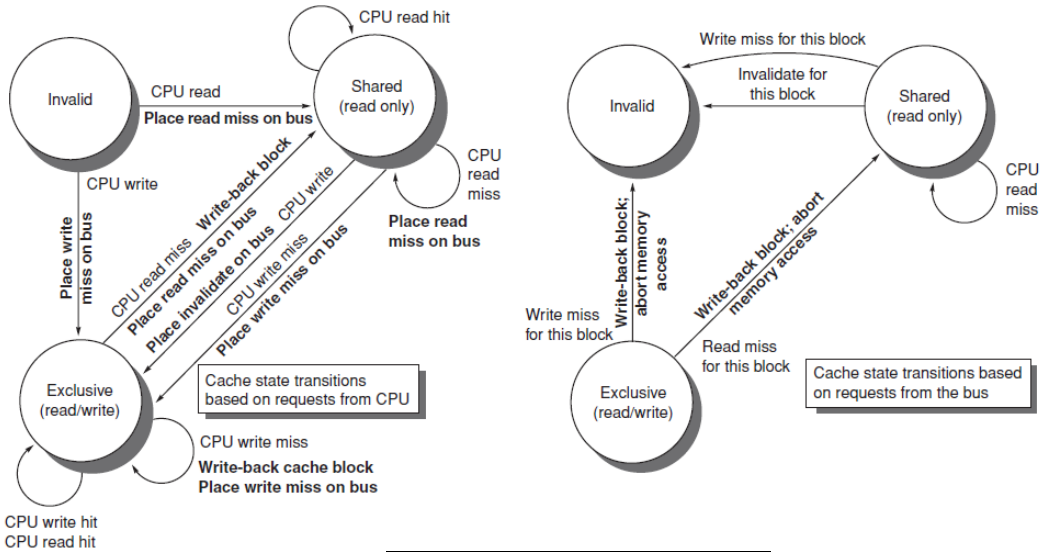
1. (10%) The term “MIPS” stands for “million instructions per second”. Computer A has a higher MIPS than computer B. Is it proper to conclude that the performance of computer A is better than computer B? Why or why not?

2. (10%) Please use a figure to illustrate a (2,2) predictor selected by the lower order 10 bits of branch address and explain how it works in details. How many bits are required in this predictor?

3. (10%)
(A) Write down an example of RAW, WAR and WAW dependencies, respectively.
(B) Please give me an example of using register renaming to eliminate WAR dependence

4. (10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 8 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?
MUL F6, F5, F6
SUB F2, F7, F8
DIV F10, F6, F5
ADD F5, F8, F2

5. (10%) For multi-processor machines, cache coherence is an important issue. The state transition diagrams of a write invalidate, cache coherence protocol for a write-back cache are illustrated below. Suppose two processors P1 and P2 are both in Shared state for a data block X. P1 writes X at time T1. Then, P2 writes X at time T2. Afterwards, P1 reads X at time T3. Please write down and explain the state transitions, bus activities, and the actions of P1 and P2 at time T1, T2, and T3.



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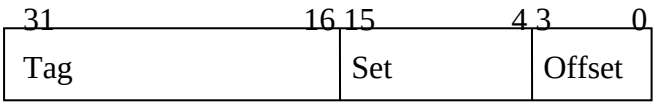
6. (18%) A 32-bit cache memory address is decomposed into 3 fields as shown as below:



A. (8 pts.) Assume the cache is 2-way set associative. What is the total size (including tag, data and valid bits) of the cache memory in bits?

B. (10 pts.) Assume that the original cache memory mentioned above is empty. Then the CPU accesses the memory with the following address sequence:

a.0x43AB1B34
b.0x43AB2810
c.0x16381B34
d.0x43AB1B3A
e.0x28CA2810
f.0x42131B35
g.0x42131B30
h.0x16381B34
i.0x43AB281C
j.0x43AB280C

If the block replacement policy is LRU. Please indicate which memory accesses (a~j) are "miss" and which (a~j) are "hit"?

7. (32%) Please answer the following questions:

A. (8 pts.) What are "microprogramming" and "hardwired control"?

B. (8 pts.) Given TLB, main memory, page table, cache and the secondary storage, please describe the procedures of a memory access by using these components.

C. (8 pts.) Please compare VLIW and superscalar machines.

D. (8 pts.) Please describe the reasons why we need memory hierarchy and how it works.