國立中央大學資訊工程學系 106 學年度第一學期博士班資格考試題紙

科目： **計算機結構** （Computer Architecture）第一頁　共二頁(page 1 of 2 ）

1. (10%) Compute the clock cycle per instruction (CPI) for the following instruction mix. The mix includes 25% loads, 18% stores, 40% R-format operations, 15% branches, and 2% jumps. The number of clock cycles for each instruction class is listed as follows. 5 cycles for loads, 4 cycles for stores, 4 cycles for R-format instructions, 4 cycles for branches, 3 cycles for jumps.

2. (10%) Briefly and clearly explain how a (m,n) correlating branch predictor works? For a (2,3) correlating branch predictor, how many branch-selected entries are there in the predictor with a total 64K bits in the prediction buffer. How many bits from the last bits of branch address are used to select the prediction entries?

3. (10%) What is Loop Unrolling when exploiting instruction level parallelism? What are the advantages? Explain it clearly by an example.

4. (10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 8 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?
MUL F6, F5, F6
SUB F2, F7, F8
DIV F10, F6, F5
ADD F5, F8, F2

5. (10%) For a disk subsystem, a redundant power supply is added to improve the dependability of the system. Suppose that the MTTF of the power supply pair is 5000 times better than one single power supply. Also, assume that fraction of the failure rate that could be improved is 15% by adding the redundant power supply. Calculate the reliability improvement that can be gained in the entire disk subsystem by adding the redundant power supply.

6. (10%) Given TLB, main memory, page table, cache and the secondary storage (disk), please describe the procedures of a memory access by using these components. (Please ensure that there should be no memory access conflict if two different programs are running simultaneously.)

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7. (10%) Assume that a computer's address size is d bits, the cache size is C bytes, the block size is B bytes, and the cache is A-way set associative. Assume that B is a power of two, so $B=2^b$. Please figure out the following quantities in terms of A, B, C, b and d.
a. The number of sets in the cache.
b. The number of index bits in the address.
c. The number of bits to implement the cache (including valid bits, tag bits and data bits.)

8. (10%) Please explain briefly the following addressing modes:
a. Registering addressing
b. Base-register addressing
c. Immediate addressing
d. PC-relative addressing
e. Direct addressing

9. (10%) In designing the memory hierarchy, please describe the positive and negative effects of increasing the cache size, associative and block size.

10. (10%) Given a processor with a base CPI of 1.0 (assuming all references hit in the primary cache) and a clock rate of 2 GHz, the main memory access time is 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 4%. How much faster will the processor be if we add a secondary cache that has a 10 ns access time for either a hit or a miss and is large enough to reduce the global miss rate happening in the main memory to 0.5%?