科目：**計算機結構**（Computer Architecture）第一頁　共二頁(page 1of 2 ）

1. (10%) Briefly and clearly explain how a (m,n) correlating branch predictor works? For a (3,2) correlating branch predictor, how many branch-selected entries are there in the predictor with a total 1024K bits in the prediction buffer. How many bits from the last bits of branch address are used to select the prediction entries?

2. (10%) What are the advantages of allowing out-of-order execution and out-of-order completion? What kind of hazards would be introduced because of out-of-order execution and out-of-order completion?

3. (10%)
   (A) Write down an example of RAW, WAR and WAW dependencies, respectively.
   (B) Please give me an example of using register renaming to eliminate WAR dependence.

4. (10%) Suppose we have the following measurements:
   Frequency of Floating Point (FP) operations = 20%
   Average CPI of FP operations = 4
   Average CPI of other instructions = 1.5
   Frequency of Floating Point Square Root (FPSQR)=5%
   CPI of FPSQR = 20
   There are two design alternatives to improve the system.
   Alternative A: to decrease the CPI of FPSQR to 2
   Alternative B: to decrease the average CPI of all FP operations to 2.
   (A) Compare these two design alternatives by calculating the average CPI of two improvement alternatives. Which alternative is better?
   (B) Use Amdahl's Law to compute the speedup of the two alternatives over the system before improvement.

5. (10%) For multi-processor machines, cache coherence is an important issue. The state transition diagrams of a write invalidate, cache coherence protocol for a write-back cache are illustrated below. Suppose two processors P1 and P2 are both in Shared state for a data block X. P1 writes X at time T1. Then, P2 writes X at time T2. Afterwards, P1 reads X at time T3. Please write down and explain the state transitions, bus activities, and the actions of P1 and P2 at time T1, T2, and T3.

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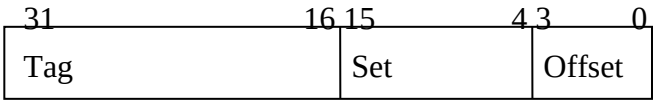
6. (40%) About memory hierarchy
   (A) Describe the reason why we need memory hierarchy and how it can work. (5 pts.)
   (B) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way. (10 pts.)
   (C) Describe the possible positive and negative effects of increasing (a) cache size, (b) associativity and (c) block size to the overall performance of memory access. (10 pts.)
   (D) Find the average memory access time (AMAT) with a 1 GHz clock, a cache access time (including hit detection) with 1 clock cycle, , a cache miss rate with 0.08 misses per instruction, a cache miss penalty with 20 clock cycles (i.e. main memory access), Assume that the read and write miss penalties are the same and ignore other write stalls. (5 pts.)
   (E) As in (D), suppose we can improve the cache miss rate to 0.05 misses per reference by doubling the cache size. This causes cache access time to increase to 1.8 cycles. Using the AMAT as a metric, determine if this is a good trade-off. (5 pts.)
   (F) As in (D), if we add another level of cache with access time 5 clock cycle, which has 20% local miss rate. Determine the AMAT. (5 pts.)

7. (10%) A 32-bit cache memory address is decomposed into 3 fields as shown as below:



Assume that the cache memory is 2-way set associative and is originally empty. Then the CPU accesses the memory with the following address sequence:

a.0x24AB1A34
b.0x24AB2810
c.0x24AC1A34
d.0x24AB1A3A
e.0x24AC2812
f.0x24AC1A35
g.0x24AA1A30
h.0x24AC1A34
i.0x24AA1A3F
j.0x24AB1A31
k.0x24AB2809
l.0x13AB2812
m.0x24AA1A40

If the block replacement policy is LRU (Least Recently Used). Please indicate which memory accesses (a~m) are “miss” and which (a~m) are “hit”?