國立中央大學資訊工程學系 105 學年度第一學期博士班資格考試題紙

科目： **計算機結構**（Computer Architecture） 第一頁 共二頁(page 1 of 2 ）

1. (10%) Explain three types of Hazards in pipelined machines using an example for each type.

2. (10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 7 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion are allowed. What hazards will be encountered when executing this code sequence?
   MUL F2, F5, F6
   ADD F2, F7, F8
   DIV F10, F2, F5
   SUB F5, F8, F2

3. (10%) Please give me an example of a loop code sequence that cannot be unrolled.

4. (10%) Suppose that FPSQR instructions are improved with speedup=10. FPSQR instructions are responsible for 10% of the execution time. What is the overall speedup?

5. (10%) Briefly and clearly explain the following terms:
   (a) Dynamic scheduling
   (b) Translation Look-aside buffer
   (c) Super-scalar processor

6. (10%) In designing the memory hierarchy, please describe the positive and negative effects of increasing the cache size, associative and block size.

7. (10%) When summarizing the performance results of a machine by running several programs of a benchmark (e.g. SPEC), will we use the geometric mean or the arithmetic mean? Why?

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8. (10%) When designing a low-power real-time embedded system, e.g., a handheld multimedia player, what control method, hardwired or microprogramming, will you use and why? In addition, in your personal opinions, how is memory hierarchy design in such a system different from the designs of desktops or servers?

9. (10%) Given a cache of 64K blocks, a 4-word block size and a 32-bit address, please find the total number of tag and index bits in the caches that are (a) direct mapped, (b) 4-way set-associative and (c) fully-associative.

10 (10%) In your opinion, what are the future directions of computer architectures and compilers?