科目：計算機結構（Computer Architecture）第一頁 共一頁(page 1 of 1)

1. (10%) Briefly and clearly explain how a (m,n) correlating branch predictor works? For a (3,2) correlating branch predictor, how many branch-selected entries are there in the predictor with a total 32K bits in the prediction buffer. How many bits from the last bits of branch address are used to select the prediction entries?

2. (10%) Describe and explain Amdahl's Law. Provide an example of calculating speedup using Amdahl's Law.

3. (15%) Briefly and clearly explain the following terms:
   (a) Virtual Memory
   (b) Translation Look-aside buffer
   (c) Dynamic scheduling

4. (15%) Compared with memory or other forms of internal storage, what are the advantages of using general purpose registers in the instruction set design?

5. (10%) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way.

6. (10%) Given a processor with a base CPI of 1.0 (assuming all references hit in the primary cache) and a clock rate of 5 GHz, the main memory access time is 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%. How much faster will the processor be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the global miss rate happening in the main memory to 0.5%?

7. (10%) Given that a memory address has 32 bits and a four-way set-associative cache which can hold 8K blocks with the block size equal to 64 bytes is used, how many "total" tag bits are there in this cache?

8. (10%) What are "forwarding" and "delayed branch" in pipelining?

9. (10%) What are 3C misses in memory hierarchy design? How can we improve or modify our design after evaluating 3C misses?