1. (10%) Compared with memory or other forms of internal storage, what are the advantages of using general purpose registers in the instruction set design?

2. (10%) Compute the clock cycle per instruction (CPI) for the following instruction mix. The mix includes 25% loads, 11% stores, 47% R-format operations, 15% branches, and 2% jumps. The number of clock cycles for each instruction class is listed as follows. 5 cycles for loads, 4 cycles for stores, 4 cycles for R-format instructions, 4 cycles for branches, 3 cycles for jumps.

3. (10%) What is Loop Unrolling when exploiting instruction level parallelism? What are the advantages? Explain it clearly by an example.

4. (10%) What is dynamic scheduling? Why is dynamic scheduling important?

5. (10%) For a disk subsystem, a redundant power supply is added to improve the dependability of the system. Suppose that the MTTF of the power supply pair is 5000 times better than one single power supply. Also, assume that fraction of the failure rate that could be improved is 20% by adding the redundant power supply. Calculate the reliability improvement that can be gained in the entire disk subsystem by adding the redundant power supply.

6. (10%) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way.

7. (10%) Please describe and compare VLIW and Superscalar processors.

8. (10%) Describe and compare microprogramming and hardwired control.

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9. (10%) You are responsible for evaluating the performances of two computers M1 and M2. M1 has a clock rate of 1GHz and M2 has a clock rate of 800MHz. The following shows the CPI of 3 instruction classes (A, B and C):

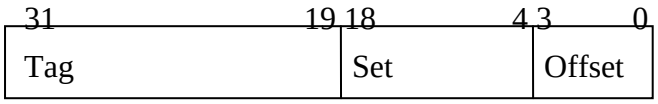
Instruction Class	CPI for M1	CPI for M2
A	3	2
B	4	4
C	4	3

There are 3 compilers: C1, C2, C3 that produce the instruction mixes as follows:

Instruction Class	C1	C2	C3
A	30%	25%	50%
B	50%	25%	30%
C	20%	50%	20%

Assume that any of the three compilers (C1, C2, C3) can be used in M1 and M2. We also assume that the numbers of instructions from C1 and C2 are the same for both M1 and M2 and equal to 1000, while the number of instructions from C3 is 1050 (for both M1 and M2). Which of the following combinations of compiler + computer will you choose?
(A) C1+M1 (B) C2+M1 (C) C3+M1 (D) C2+M2 (E) C3+M2

10. (10%) A 32-bit cache memory address is decomposed into 3 fields as :



Assume the cache is 4-way set associative. What is the total size (including tag and data bits but excluding other valid/dirty bits) of the cache memory in **bits**?