

科目：計算機結構 (Computer Architecture) 第一頁 共二頁 (page 1 of 2)

1. (15%) Consider the following code

SUB R2, R1, R3

LD R1, 100(R2)

ADD R2, R1, R3

What kind of hazard would happen if there is no forwarding mechanism? Please specify that the data hazard would happen between which instructions? And due to which registers? Write down the logic to detect all the data hazards and determine where the forwarding mechanism is needed. If there is forwarding mechanism implemented, would there still be data hazard?

2. (15%) Briefly and clearly explain how a (m,n) correlating branch predictor works? For a (3,2) correlating branch predictor, how many branch-selected entries are there in the predictor with a total 32K bits in the prediction buffer. How many bits from the last bits of branch address are used to select the prediction entries?
3. (10%) What is Loop Unrolling when exploiting instruction level parallelism? What are the advantages? Explain it clearly by an example.
4. (10%) Suppose that Floating point instructions are improved with speedup=5. Only 20% of actual instruction execution time is contributed by Floating Point instructions. What is the overall speedup?

5. (15%) Consider two different implementations of the same instruction set architecture. There are five classes of instructions, A, B, C, D and E. The clock rate and the CPI of each implementation are given in the following table.

	ClockRate	CPIA	CPIB	CPIC	CPID	CPIE
P1	2. G	1	2	3	5	4
P2	1.8G	3	3	3	3	3

- (1) Given a program with 10^5 instructions divided into classes as follows: 10% Class A, 15% Class B, 40% Class C, 20% Class D and 15% Class E. Which one is fast by their MIPS? Is MIPS a reasonably reliable metric in this case? (10 pts.)
- (2) Following (1), you are trying to improve P1 by saving 20% in the execution time. However, this leads to an increase of 20% of the average CPI. What clock rate should we have to set to achieve this time reduction? (5 pts.)

6. (35%) About memory hierarchy
- (1) Describe the reason why we need memory hierarchy and how it can work. (5 pts.)
 - (2) Given cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way. (10 pts.)
 - (3) Describe the possible positive and negative effects of increasing (a) cache size, (b) associativity and (c) block size to the overall performance of memory access. (10 pts.)
 - (4) Find the average memory access time (AMAT) with a 1 ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.08 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls. (5 pts.)
 - (5) As in (3), suppose we can improve the miss rate to 0.05 misses per reference by doubling the cache size. This causes access time to increase to 1.8 cycles. Using the AMAT as a metric, determine if this is a good trade-off. (5 pts.)