1. (10%) Given TLB, main memory, page table, cache and the secondary storage (disk), please describe the procedures of a memory access by using these components.

2. (14%) You are designing a low-power real-time embedded system, say a handheld multimedia player
   (a) (7%.) What control method, hardwired or microprogramming, will you use and why?
   (b) (7%) In your personal opinions, how is memory hierarchy design in such a system different from the designs of desktops or servers?

3. (12%) Given a cache of 32K blocks, a 4-word block size and a 32-bit address, please find the *total* number of tag and index bits in the caches that are (a) direct mapped, (b) 4-way set-associative and (c) fully-associative.

4. (14%) You are responsible for purchasing a computer system for your lab. There are two choices: M1 and M2.

Instruction class	CPI for M1	CPI for M2
A	4	2
B	6	4
C	8	3

The machine M1 has a clock rate of 4GHz and M2 has a clock rate of 2GHz.
Consider the following compilers C1, C2 and C3 that produce the instruction frequency shown below:

Instruction class	C1	C2	C3
A	30%	30%	50%
B	50%	20%	30%
C	20%	50%	20%

   (a) (7%) For the compiler C1, which processor (M1 or M2) is faster and by how much?
   (b) (7%) Assuming that any of the three compilers can be used on M1 and M2, which of these two machines and which compiler should be purchased?

5. (10%) If modules have exponentially distributed lifetimes (age of module does not affect probability of failure), the overall failure rate is the sum of failure rates of the all modules in a system. A disk subsystem contains the following components: 16 disks (1M hour MTTF per disk), 1 disk controller (1M hour MTTF), and 1 power supply (1M hour MTTF). 1 fan (1M hour MTTF), 1 SCSI cable (1M hour MTTF)
   (A) Calculate MTTF for the disk subsystem
   (B) Assume that after adding one redundant power supply, the reliability of the power supply improves about 1000 times. What is the reliability improvement of the entire disk subsystem?

6. (10%) Consider the following instruction mix and clock cycle per instruction:
   - Frequency of ALU instructions: 40%
   - Frequency of data transfer instructions: 30%
   - Frequency of branch instructions: 30%
   - ALU instructions take 2 cycles, data transfer instructions take 3 cycles, branch instructions take 3 cycles.

   There are two enhancement alternatives:
   Enhancement A: reduce ALU instructions to 1 cycle.
   Enhancement B: reduce branch instructions to 2 cycles.
   (a) Calculate the CPI for each enhancement alternatives.
   (b) Calculate the speedup for each enhancement using **Amdahl's law**.

7. (10%) Considering the following code sequence,

```
LOAD    R1, 45(R2)
SUB     R3, R2, R1
LOAD    R2, 50(R1)
ADD     R1, R2, 100
OR      R3, R2, R1
```

   (1) What are the logic detecting the data hazard conditions of the load interlocks?

	Opcode field of ID/EX ($ID/EX.IR_{0..5}$)	Opcode field of IF/ID ($IF/ID.IR_{0..5}$)	Matching operand fields
(Rule 1)	Load	Register-register ALU	ID/EX.IR[rt] == IF/ID.IR[rs]
(Rule 2)	Load	Register-register ALU	ID/EX.IR[rt] == IF/ID.IR[rt]
(Rule 3)	Load	Load, store, ALU immediate, or branch	ID/EX.IR[rt] == IF/ID.IR[rs]

   (A) Rule 1 and Rule 2
   (B) Rule 2 and Rule 3
   (C) Rule 3 and Rule 1
   (D) Rule 3
   (E) Rule 1

   (2) Is forwarding necessary between the first LOAD and the SUB instruction? If yes, what is the logic detecting the forwarding condition between the first LOAD and the SUB? Detection Logic Options for (2):

	Pipeline register containing source instruction	Opcode of source instruction	Pipeline register containing destination instruction	Opcode of destination instruction	Destination of the forwarded result	Comparison (if equal then forward)
(A)	EX/MEM	Register-register ALU	ID/EX	Register-register ALU, ALU immediate, load, store, branch	Top ALU input	EX/MEM.IR[rd] == ID/EX.IR[rs]
(B)	EX/MEM	Register-register ALU	ID/EX	Register-register ALU	Bottom ALU input	EX/MEM.IR[rd] == ID/EX.IR[rt]
(C)	MEM/WB	Register-register ALU	ID/EX	Register-register ALU, ALU immediate, load, store, branch	Top ALU input	MEM/WB.IR[rd] == ID/EX.IR[rs]
(D)	MEM/WB	Register-register ALU	ID/EX	Register-register ALU	Bottom ALU input	MEM/WB.IR[rd] == ID/EX.IR[rt]
(E)	EX/MEM	ALU immediate	ID/EX	Register-register ALU, ALU immediate, load, store, branch	Top ALU input	EX/MEM.IR[rt] == ID/EX.IR[rs]
(F)	EX/MEM	ALU immediate	ID/EX	Register-register ALU	Bottom ALU input	EX/MEM.IR[rt] == ID/EX.IR[rt]
(G)	MEM/WB	ALU immediate	ID/EX	Register-register ALU, ALU immediate, load, store, branch	Top ALU input	MEM/WB.IR[rt] == ID/EX.IR[rs]
(H)	MEM/WB	ALU immediate	ID/EX	Register-register ALU	Bottom ALU input	MEM/WB.IR[rt] == ID/EX.IR[rt]
(I)	MEM/WB	Load	ID/EX	Register-register ALU, ALU immediate, load, store, branch	Top ALU input	MEM/WB.IR[rt] == ID/EX.IR[rs]
(J)	MEM/WB	Load	ID/EX	Register-register ALU	Bottom ALU input	MEM/WB.IR[rt] == ID/EX.IR[rt]

8. (10%) Assume a write invalidate cache coherence protocol for a write-back cache. Suppose three processors P1, P2, and P3 are in Shared state for a data block X. P1 writes X at time T1. Then, P2 reads X at time T2. Afterwards, P3 writes X at time T3. Please write down and explain the state transitions, bus activities and actions of P1 P2 and P3 at time T1, T2, and T3.

9. (10%) (a) How many entries are there in a (3,2) correlating predictor with total 512K bits in the branch prediction buffer? (b) How many lower order address bits are used to index the branch prediction buffer?