國立中央大學資訊工程學系 113 學年度第一學期博士班資格考試題紙

科目： **計算機結構**（Computer Architecture） 第一頁 共兩頁(page 1 of 2）

1. (10%)
   (1) (5%) Why is dynamic scheduling important?
   (2) (5%) Please explain SIMD (Single Instruction stream Multiple Data stream). What are the applications suitable for it?

2. (10%) Which of the following statements are true for scoreboard?
   (A) Scoreboard allows out-of-order issuing.
   (B) Scoreboard allows out-of-order execution.
   (C) Scoreboard allows the instructions to be completed out of order.
   (D) Scoreboard checks for structural hazard before issuing the instructions.
   (E) Scoreboard checks for WAW hazard when writing back the result.

3. (10%) Which of the following statements are true for General-purpose register (GPR) instruction architecture?
   (A) One of the advantages of register-register instructions is simple code-generation.
   (B) The instruction count for register-register instructions is usually lower than register-memory instructions.
   (C) Using registers is more efficient for a compiler than other forms of internal storage.
   (D) When variables are allocated to registers, the memory traffic reduces, the program speeds up.
   (E) None of the above.

4. (10%) What is a loop-carried dependence? Please give me an example of a loop code sequence that cannot be unrolled.

5. (10%) Consider the following code sequence. F1- F10 are registers. Assume the following execution time for different operations: MUL takes 8 cycles, DIV takes 20 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?
   MUL F6, F5, F6
   SUB F2, F7, F8
   DIV F10, F6, F5
   ADD F5, F8, F2

背面還有 Please Turn Over

6. (15%) About memory hierarchy
   (1) (7%) What is locality? And then explain why memory hierarchy can help to improve the performance by employing locality.
   (2) (8%) What are 3C misses in memory design? How can we improve or modify our design after evaluating 3C misses?

7. (15%) Assume that we have a 32-bit processor (with 32-bit words) and that this processor is byte-addressed. Suppose that it has a 128-byte (32-word) cache that is two-way set associative, has 4 words in a block, and uses LRU replacement algorithm.
   (1) (7%) Split the 32-bit address into 4 parts: "tag", "index", "block" and "byte" offset. Which address bits comprise each part?
   (2) (8%) Here is a series of address references given as word addresses: 1, 4, 8, 5, 17, 32, 19, 1, 56, 9, 25. Label each reference in the list as hit or miss and show the final content of the cache. (Note: The first word address of each block is a multiple of 4.)

Address	1	4	8	5	17	32	19	1	56	9	25
Hit/Miss											

8. (10%) Which of the following statement(s) should be true?
   (A) There are more addressing modes in RISC than in CISC.
   (B) Microprogramming is usually used in RISC since this kind of control can be executed faster.
   (C) Vertical microinstructions are executed faster than Horizontal microinstructions.
   (D) Using ROM in the control designs can usually save the space or cost, when compared with PLA.
   (E) None of the above is true.

9. (10%) Consider two different implementations of the same instruction set architecture. There are five classes of instructions, A, B, C, D and E. The clock rate and the CPI (cycles per instruction) of each implementation are given in the following table.

	Clock Rate	CPI_A	CPI_B	CPI_C	CPI_D	CPI_E
P1	2.0G	1	2	3	5	4
P2	1.8G	3	3	3	3	3

   (1) (5%) Given a program with 10^5 instructions divided into classes as follows: 10% Class A, 15% Class B, 40% Class C, 20% Class D and 15% Class E. Which implementation (P1 or P2) is faster?
   (2) (5%) Following (1), you are trying to improve P1 by saving 20% in the execution time. However, this leads to an increase of 15% of the average CPI. What clock rate should we have to set to achieve this time reduction?