國立中央大學資訊工程學系 110 學年度第二學期博士班資格考試題紙

科目： **計算機結構** （Computer Architecture） 第一頁 共一頁(page 1 of 1 ）

1. (10%) Strip mining is a technique that generates codes such that each vector operation is done for a size less than or equal to the maximum vector length. Please explain why we need it in a vector architecture.

2. (10%) Describe three techniques that can reduce miss rate? Explain each method clearly.

3. (10%) What are the characteristics and advantages of Reduced Instruction Set Computer (RISC) Architecture?

4. (10%) What are the bottlenecks for improving uniprocessor performance?

5. (10%) Hardware-based speculation

(a) What is the concept of hardware-based speculation?

(b) What additional hardware is required to support hardware-based speculation?

6. (10%) Given the cache, TLB, page table, main memory and the secondary storage (disk), describe the process of a memory access in a systematical way.

7. (10%) The CPI of a machine without any memory stall is 1.2. Assume that the instruction mix is 50% ALU, 30% data memory-access and 20% control. Now, 10% of data memory-access instructions will cause misses with the penalty 50 clock cycles. Besides, 1% of miss will also happen in the instruction memory with the penalty 50 clock cycles. Please calculate the resulting CPI.

8. (10%) Given a cache of 128K blocks, a 128-byte block size and a 32-bit address, please find the total number of tag bits in the caches that are (a) direct mapped, (b) 2-way set-associative and (c) fully-associative.

9. (10%) True of False (A wrong answer will cause one more point loss.)

(a) A common way of presenting computer performance in a benchmark is to normalize execution times to a reference computer. Then the arithmetic mean is usually used to ensure that the evaluation will not be affected by using different reference machines.

(b) In the history of computers' development, the size of memory and number of registers in a computer grow according to the Moore's law.

(c) For a little-endian machine, if we write a 32-bit (4-byte) data word, 0xABCDEFCD, to the address 0x8000, then the byte at 0x8000 is 11001101.

(d) Tera bytes indicate 2^{40} bytes. Three Pico seconds indicate $3x10^{-12}$ seconds.

(e) Superscalar machines achieve the instruction parallelism mainly by hardware.

10. (10%) When designing a low-power real-time embedded system, what control method, hardwired or microprogramming, will you use and why? In addition, how is memory hierarchy design in such a system different from the designs of desktops or servers?